IN THE CLAIMS

Please amend the claims as follows:

Claims 1-143 (Canceled)

144 - 148. (Cancelled)

149. (Previously presented) An integrated circuit comprising:

a monocrystalline silicon substrate;

a first accommodating buffer layer comprising an amorphous oxide material in contact with the monocrystalline silicon substrate and a monocrystalline metal oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide and mixtures thereof contacting the amorphous oxide material;

a first monocrystalline semiconductor layer overlying the first accommodating buffer layer;

a second accommodating buffer layer comprising an amorphous oxide material and a monocrystalline metal oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide and mixtures thereof contacting the amorphous oxide material overlying the first monocrystalline semiconductor layer; and

a second monocrystalline semiconductor layer overlying the second accommodating buffer layer.

150. (Previously Presented) The integrated circuit of claim 149, wherein:

one of the first and second monocrystalline semiconductor layers is a monocrystalline compound semiconductor layer; and

the other of the first and second monocrystalline semiconductor layers is a monocrystalline Group IV semiconductor layer.

151. (Previously Presented) The integrated circuit of claim 149, wherein:
the first monocrystalline semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the first accommodating buffer layer;
the second accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the first monocrystalline semiconductor layer; and
the second monocrystalline semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the second accommodating buffer layer.

152. (Previously Presented) The integrated circuit of claim 149, wherein:
the first accommodating buffer layer and the first monocrystalline semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the first monocrystalline semiconductor layer is at least approximately 20 nm; and
the second accommodating buffer layer and the second monocrystalline semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the second monocrystalline semiconductor layer is at least approximately 20 nm.

153. (Previously Presented) The integrated circuit of claim 149, further comprising a monocrystalline Group IV substrate underlying the first accommodating buffer layer.

154. (Previously Presented) An integrated circuit comprising:
a monocrystalline silicon substrate;
an accommodating buffer layer comprising an amorphous oxide material in contact with the monocrystalline silicon substrate and a monocrystalline metal oxide selected from the group consisting of alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates,

alkaline earth metal niobates, alkaline earth metal vanadates, alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, gadolinium oxide and mixtures thereof contacting the amorphous oxide material; and

active devices, wherein all the active devices lie at least partially within or over a monocrystalline compound semiconductor layer that overlies the accommodating buffer layer.

155. (Previously Presented) The integrated circuit of claim 154, wherein:

the integrated circuit includes electronic components;

the electronic components include the active devices active and at least one other component; and

all the electronic components lie at least partially within or over a monocrystalline compound semiconductor layer that overlies the accommodating buffer layer.

156. (Previously Presented) The integrated circuit of claim 154, wherein the compound semiconductor layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the accommodating buffer layer.

157. (Cancelled)

158. (Previously Presented) The integrated circuit of claim 154, wherein the substrate that is at least approximately 300 millimeters wide.

159. (Previously Presented) The integrated circuit of claim 154, wherein the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the substrate.

160. (Previously Presented) The integrated circuit of claim 154, wherein the integrated circuit has at least one feature selected from the group consisting of:

the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the substrate; and

the accommodating buffer layer and the substrate have a lattice mismatch no greater than approximately 2.0% and a thickness of the accommodating buffer layer is at least approximately 20 nm.

161. (Previously Presented) The integrated circuit of claim 154, wherein:
the accommodating buffer layer has a crystal orientation that is rotated by approximately 45° with respect to a crystal orientation of the substrate; and
the accommodating buffer layer and the monocrystalline Group IV semiconductor substrate have a lattice mismatch no greater than approximately 2.0% and a thickness of the accommodating buffer layer is at least approximately 20 nm.

162. (Previously Presented) The integrated circuit of claim 154, wherein the accommodating buffer layer and the monocrystalline compound semiconductor layer have a lattice mismatch no greater than approximately 2.0% and a thickness of the monocrystalline compound semiconductor layer is at least approximately 20 nm.